JL7016C Datasheet

JIELI TECHNOLOGY

Zhuhai Jieli Technology Co.,LTD

Version：1.0

Date：2022.04.15

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JL7016C Features

CPU

- 32bit Dual-Core DSP
- Maximum speed 160MHz
- 32KB ICache and 16KB DCache
- IEEE754 Single precision FPU
- Mathematical accelerate engine
- Interrupts with 8 priority level

Memory

- On-chip 640KB SRAM
- Support MMU
- Built-In Flash

Clocks

- On-chip 16 MHz clock oscillator
- On-chip 200 kHz lower-temperature-drift clock oscillator
- 24 MHz crystal oscillator
- 32.768 kHz crystal oscillator

DSP Audio Processing

- SBC/mSBC encoder and decoder
- Support MP2, MP3, WMA, APE, FLAC, AAC, MP4, M4A, WAV, AIF, AIFC audio decoding
- Packet Loss Concealment (PLC) for voice processing
- Single/Dual MIC Environmental Noise Cancellation (ENC)
- Multi-band DRC limiter
- Multi-band EQ configuration for voice Effects

Audio Codec

- Two channels 24-bit DAC,
  SNR ≥ 98dB (Single-ended)
  SNR ≥ 104dB (Differential)
- Four channels 24-bit ADC,SNR ≥ 95dB
- Audio DAC Sampling rates of 8kHz/11.025kHz/16kHz/22.05kHz/24kHz/ 32kHz/44.1kHz/48kHz/64kHz/88.2kHz/ 96kHz are supported
- Audio ADC Sampling rates of 8kHz/11.025kHz/16kHz/22.05kHz/24kHz/ 32kHz/44.1kHz/48kHz are supported
- Support four digital/analog MIC inputs
- Four channels analog audio inputs
- Audio DAC support differential cap-less mode or single-ended mode
- Direct drive 16ohm/32ohm Speaker loading

Bluetooth

- Compliant with Bluetooth V5.3+BR+EDR+BLE specification
- Support AoA/AoD direction finding
- Support LE audio BIS/CIS full function
- Meet class2 and class3 transmitting power requirement
- Maximum +9dbm transmitting power
- EDR receiver with minimum -95dBm sensitivity
- Support a2dp\avctp\avdtp\avrcp\hfp\spp\smp\ att\gap\gatt\rfcomm\sdp\l2cap profile
- bap 1.0\pacs 1.0\ccp 1.0\mcp 1.0\micp 1.0\vcp 1.0\csip 1.0
- a2dp 1.3.2\avctp 1.4\avdtp 1.3\ avrcp 1.6.2\hfp 1.8 \spp 1.2\rfcomm 1.1\pnp 1.3\hid 1.1.1\sdp core5.3\l2cap core 5.3

Peripherals

- One full speed USB OTG controller
- One SD host controller for eMMC/SD
- Six multi-function 32-bit timers, support capture and PWM mode
- UART interface
- I2C Master/Slave interface
- SPI Master/Slave interface
- I2S Master/Slave interface
- QDEC
- Low power CapSense
- 11-channel 10-bit ADC for analog sampling
- Motor PWM controller

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- 22 Individually programmable and multiplexed GPIO pins
- Up to 12 external interrupt/wake-up source(low power available,can be multiplexed to any I/O)

PMU

- Built-in lithium battery charging manager,up to 200mA charging current
- Less than 2uA sleep current
- VPWR range : 4.5V to 5.5V
- VBAT range : 2.2V to 4.5V
- IOVDD range : 2.2V to 3.6V

Packages

- QFN32(4mm*4mm)

Temperature

- Operating temperature: -40℃ to +85℃
- Storage temperature: -65℃ to +150℃

Applications

- Bluetooth Stereo speaker
- Bluetooth Rod speaker

1、Pin Definition

1.1 Pin Assignment

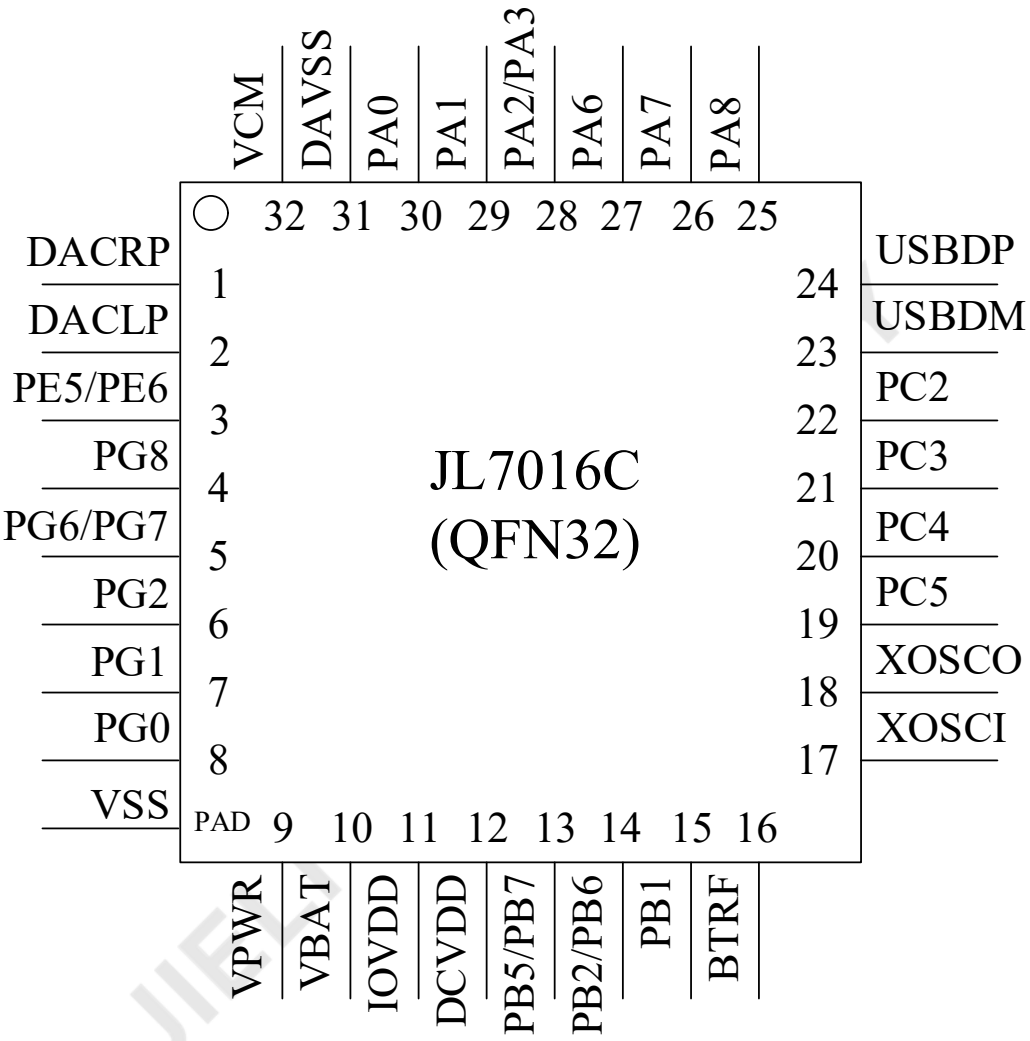


Figure 1-1 JL7016C Package Diagram

1.2 Pin Description

Table 1-1 JL7016C Pin Description

PIN NO.	Name	Type	Function	Other Function
1	DACRP	AO		Right channel audio output positive;
2	DACLP	AO		Left channel audio output positive;
3	PE5	I/O	GPIO	
	PE6	I/O	GPIO	SDPG:SD card power gate;
4	PG8	I/O	GPIO	MICIN2:MIC2 Input Channel 2; MIC2_P:Different MIC2 Positive; AMUX_C0:Analog Channel C0 input；
5	PG6	I/O	GPIO	LCD_SPID2(B); MICIN3:MIC3 Input Channel 3; MIC3_P:Different MIC3 Positive; AMUX_D0:Analog Channel D0 input； FPIN2;
	PG7	I/O	GPIO	LCD_SPID3(B); MIC_BIAS2:MIC2 Bias Output(Built-in resistor); MIC2_N:Different MIC2 Negative; AMUX_C1:Analog Channel C1 input； ADC15:ADC Input Channel 15;
6	PG2	I/O	GPIO	TDM_DAT; SFC_DAT2B(2):SFC Data2 Out(B); SPI0_DAT2B(2):SPI0 Data2 Out(B); SD0_CLKB:SD0 Clock(B); PWMCH2L:Motor PWM Channel2(L);
7	PG1	I/O	GPIO	TDM_SYN; SD0_CMDB:SD0 CMD(B); ADC13:ADC Input Channel 13; PWMCH2H:Motor PWM Channel2(H);
8	PG0	I/O	GPIO	TDM_CLK; LVD:Low Voltage Detect; SD0_DATB:SD0 Data(B); ADC12:ADC Input Channel 12; TMR2CK;
9	VPWR (PP0)	PI (I/O)	GPIO (High Voltage Resistant)	Charging power input; UART0TXB:Uart0 Data Output(B); UART0RXB:Uart0 Data Input(B); CAP1:Timer1 Capture; PWM3:Timer3 PWM Output;
10	VBAT	P		Battery interface;

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11	IOVDD	PO		Built-in linear voltage regulator output;
12	DCVDD	P		Internal power;
13	PB5	I/O	GPIO (High Voltage Resistant)	LP_Touch4:Low Power Touch Channel 4; IIC1_SDA_A:IIC1 SDA(A); ADC8:ADC Input Channel 8; UART3RXB:Uart3 Data Input(B);
	PB7	I/O	GPIO (High Voltage Resistant)	OSC32KI:32.768khz crystal oscillator input;
14	PB2	I/O	GPIO (High Voltage Resistant)	LP_Touch2:Low Power Touch Channel 2; ADC7:ADC Input Channel 7; UART3TXA:Uart3 Data Input(A);
	PB6	I/O	GPIO (High Voltage Resistant)	OSC32KO:32.768khz crystal oscillator output; PWM2:Timer2 PWM Output;
15	PB1	I/O	GPIO (pull up) (High Voltage Resistant)	Hold down 0 to reset; LP_Touch1:Low Power Touch Channel 1; ADC6:ADC Input Channel 6;
16	BTRF	RFI		Bluetooth RF antenna interface;
17	XOSCI	I		System Crystal Oscillator Input;
18	XOSCO	O		System Crystal Oscillator Output;
19	PC5	I/O	GPIO	SFC1_D2:SFC1 Data2 Out(nor flash); SPI0_DAT2C(2):SPI0 Data2 Out(C); SD0_CLKA:SD0 Clock(A); SPI1DOB:SPI1 Data Out(B); IIC0_SDA_B:IIC0 SDA(B); ALNK_DAT3(B):Audio Link Data3(B); ADC5:ADC Input Channel 5; UART2RXA:Uart2 Data Input(A);
20	PC4	I/O	GPIO	SFC1_DI(D1):SFC1 Data In(nor flash); SPI0_DIC(1):SPI0 Data In(C); SD0_CMDA:SD0 CMD(A); SPI1CLKB:SPI1 Clock(B); IIC0_SCL_B:IIC0 SCL(B); ALNK_DAT2(B):Audio Link Data2(B); ADC4:ADC Input Channel 4; UART2TXA:Uart2 Data Output(A); PWM4:Timer4 PWM Output;

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21	PC3	I/O	GPIO	SFC1_CS:SFC1 Chip Select(nor flash); LNA_EN:LNA Enable; SPI0_CSC:SPI0 Chip Select(C); SD0_DATA:SD0 Data(A); SPI1DIB:SPI1 Data In(B); ALNK_LRCK(B):Audio Link Word Select(B); TMR3:Timer3 Clock Input;
22	PC2	I/O	GPIO	SFC1_DO(D0):SFC1 Data Out(nor flash); PA_EN:PA Enable; SPI0_DOC(0):SPI0 Data Out(C); ALNK_SCLK(B):Audio Link Serial Clock(B); TMR1:Timer1 Clock Input;
23	UDBDM	I/O	USB Negative Data (pull down)	SPI2DOB:SPI2 Data Out(B); IIC0_SDA_A:IIC0 SDA(A); ADC11:ADC Input Channel 11; UART1RXB:Uart1 Data Input(B);
24	USBDP	I/O	USB Positive Data (pull down)	SPI2CLKB:SPI2 Clk(B); IIC0_SCL_A:IIC0 SCL(A); ADC10:ADC Input Channel 10; UART1TXB:Uart1 Data Output(B);
25	PA8	I/O	GPIO	LCD_SPID0/DO(A); PLNK_DAT1/ANCDE; ALNK_LRCK(A):Audio Link Word Select(A); ADC3:ADC Input Channel 3; UART2RXB:Uart2 Data Input(B);
26	PA7	I/O	GPIO	LCD_SPICLK(A); ALNK_SCLK(A):Audio Link Serial Clock(A); UART2TXB:Uart2 Data Output(B); TMR0:Timer0 Clock Input;
27	PA6	I/O	GPIO	PLNK_DAT0/ANCDR; SPI2DOA:SPI2 Data Out(A); ALNK_DAT3(A):Audio Link Data3(A); ADC2:ADC Input Channel 2; UART0RXA:Uart0 Data Input(A); CAP0:Timer0 Capture;
28	PA2	I/O	GPIO	MIC_BIAS0:MIC0 Bias Output(Built-in resistor); MIC0_N:Different MIC0 Negative; AMUX_A1:Analog Channel A1 input； CLKOUT1:Clock Out1; SPI1CLKA:SPI1 Clk(A); ALNK_MCLKA:ALNK Master Clock(A); UART1RXA:Uart1 Data Input(A); CAP3:Timer3 Capture;

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	PA3	I/O	GPIO	MICIN1:MIC1 Input Channel 1; MIC1_P:Different MIC1 Positive; AMUX_B0:Analog Channel B0 input； SPI1DOA:SPI1 Data Out(A); ALNK_DAT0(A):Audio Link Data0(A); PWM1:Timer1 PWM Output;
29	PA1	I/O	GPIO	MICIN0:MIC0 Input Channel 0; MIC0_P:Different MIC0 Positive; AMUX_A0:Analog Channel A0 input； SPI1DIA:SPI1 Data In(A); UART1TXA:Uart1 Data Output(A); PWM0:Timer0 PWM Output;
30	PA0	I/O	GPIO	MICLDO:Microphone linear voltage regulator output; ADC0:ADC Input Channel 0;
31	DAVSS	G		Audio analog ground;
32	VCM	P		Audio analog reference bias;
PAD	VSS	G		System ground;

Pin Type	**Description**	**Pin Type**	**Description**
P	Power	I/O	Input or Output
PO	Power Output	I	Input
PI	Power Input	O	Output
G	Ground	RFI	Radio frequency interface
AO	Analog Output		

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2、Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1

Symbol	Parameter	Min	Max	Unit
Topt	Operating temperature	-40	+85	°C
Tstg	Storage temperature	-65	+150	°C
VBAT	Supply Voltage	-0.3	4.5	V
VPWR	Charger Voltage	-0.3	6	V
V_{IOVDD}	Voltage applied at IOVDD	-0.3	3.6	V
V_{GPIO}	Voltage applied to GPIO	-0.3	IOVDD+0.3	V
V_{HVIO}	Voltage applied to High Voltage Resistant IO	-0.3	+5.5	V

Note : The chip can be damaged by any stress in excess of the absolute maximum ratings listed below

2.2 PMU Characteristics

Table 2-2

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VBAT	Voltage Input	2.2	3.7	4.5	V	
VPWR	Charger supply Voltage	4.5	5.0	5.5	V	
Operating mode						
IOVDD	Voltage output	2.0	3.0	3.4	V	VBAT = 4.2V, 10mA loading
	Loading current	_	_	120	mA	IOVDD=3V@VBAT = 4.2V
DCVDD	Voltage output	1.0	1.25	1.4	V	IOVDD=3.0V, 10mA loading
	Loading current	_	_	100	mA	DCVDD=1.25V@IOVDD=3.0v On LDO mode
V_{LVD}	Voltage input	1.8	2.5	2.5	V	Low-Voltage Detection for IOVDD
Low Power mode						
IOVDD	Loading current	_	_	10	mA	IOVDD=3V@VBAT = 4.2V

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2.3 Battery Charge

Table 2-3

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VPWR	Charge Input Voltage	4.5	5	5.5	V	_
$V_{bat\ float}$	Charge Voltage	4.15	4.2	4.25	V	VPWR＞4.5V
		4.30	4.35	4.40	V	VPWR＞4.65V
I_{bat}	Charge Current	15	_	200	mA	Charge current at fast charge mode VBAT=4.0V@VPWR=5.0V
I_{end}	End Of Charge Current	2	_	30	mA	End of charge current
V_{Trikl}	Trickle Charge Voltage	_	3.0	_	V	VPWR＞4.5V
I_{Trikl}	Trickle Charge Current	1.5	_	30	mA	V_{BAT}<V_{Trikl}

2.4 IO Input/Output Electrical Logical Characteristics

Table 2-4

GPIO input characteristics						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
V_{IL}	Low-Level Input Voltage	-0.3	_	0.3* IOVDD	V	IOVDD = 3.0V
V_{IH}	High-Level Input Voltage	0.7* IOVDD	_	IOVDD+0.3	V	IOVDD = 3.0V
High Voltage Resistant IO input characteristics						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
V_{IL}	Low-Level Input Voltage	-0.3	_	0.3* IOVDD	V	IOVDD = 3.0V
V_{IH}	High-Level Input Voltage	0.7* IOVDD	_	+5V	V	IOVDD = 3.0V
GPIO & High Voltage Resistant IO output characteristics						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
V_{OL}	Low-Level Output Voltage	_	_	0.1* IOVDD	V	IOVDD = 3.0V
V_{OH}	High-Level Output Voltage	0.9* IOVDD	_	_	V	IOVDD = 3.0V

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2.5 Internal Resistor Characteristics

Table 2-5

Port	Drive Current		Internal Pull-Up Resistor	Internal Pull-Down Resistor	Comment
PA PC2~PC5 PG PE5,PE6	HD,HD0==0,0	2.4mA	10K	10K	1、PB1 default pull up 2、USBDM & USBDP default pull down 3、internal pull-up/pull-down resistance | accuracy ±20%
	HD,HD0==0,1	8mA			
	HD,HD0==1,0	26mA			
	HD,HD0==1,1	46mA			
PB PP0(VPWR)	8mA (High Voltage Resistant)		10K	10K	
USBDP	4mA		1.5K	15K	
USBDM	4mA		180K	15K	

2.6 Audio DAC Characteristics

Table 2-6

Parameter	MODE	Min	Typ	Max	Unit	Test Conditions
Frequency Response		20	_	20K	Hz	1KHz/0dB 10k ohm loading With A-Weighted Filter
Output Swing	Differential		1		Vrms	
	Single-ended	_	520	_	mVrms	
THD+N	Differential	_	-70	_	dB	
	Single-ended	_	-70	_	dB	
S/N	Differential	_	104	_	dB	
	Single-ended	_	98	_	dB	
Crosstalk	Single-ended	_	90	_	dB	
Dynamic Range	Differential	_	104	_	dB	1KHz/-60dB 10k ohm loading With A-Weighted Filter
	Single-ended	_	98	_	dB	
Noise Floor	Differential	_	5.8	_	uVrms	A-Weighted Filter
	Single-ended	_	5.8	_	uVrms	

2.7 Audio ADC Characteristics

Table 2-7

Parameter	Min	Typ	Max	Unit	Test Conditions
Dynamic Range		94		dB	Fsample=44.1kHz,Gain=0dB Fin=1KHz 590mVrms
S/N	_	95	_	dB	Fsample=44.1kHz,Gain=0dB Fin=1KHz 590mVrms
THD+N	_	-75	_	dB	
S/N	_	76	_	dB	Fsample=44.1kHz,Gain=18dB

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THD+N	_	-73	_	dB	Fin=1KHz 75mVrms

2.8 BT Characteristics

2.8.1 Transmitter

Basic Data Rate **Table 2-8**

Parameter		Min	Typ	Max	Unit	Test Conditions
RF Transmit Power			7.0	9.0	dBm	25℃, Power Supply VBAT=3.7V 2441MHz
RF Power Control Range			18.2		dB	
20dB Bandwidth			950		KHz	
Adjacent Channel Transmit Power	+2MHz		-28		dBm	
	-2MHz		-34		dBm	
	+3MHz		-30		dBm	
	-3MHz		-43		dBm	

Enhanced Data Rate **Table 2-9**

Parameter		Min	Typ	Max	Unit	Test Conditions
Relative Power			-2.5		dB	25℃, Power Supply VBAT=3.7V 2441MHz
π/4 DQPSK Modulation Accuracy	DEVM RMS		6		%	
	DEVM 99%		11		%	
	DEVM Peak		16		%	
Adjacent Channel Transmit Power	+2MHz		-28		dBm	
	-2MHz		-34		dBm	
	+3MHz		-30		dBm	
	-3MHz		-43		dBm	

2.8.2 Receiver

Basic Data Rate **Table 2-10**

Parameter		Min	Typ	Max	Unit	Test Conditions
Sensitivity			-92		dBm	25℃, Power Supply VBAT=3.7V 2441MHz DH5
Co-channel Interference Rejection			10		dB	
Adjacent Channel Interference Rejection	+1MHz		-4		dB	
	-1MHz		-3		dB	
	+2MHz		-39		dB	
	-2MHz		-29		dB	
	+3MHz		-45		dB	

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	-3MHz		-23		dB	

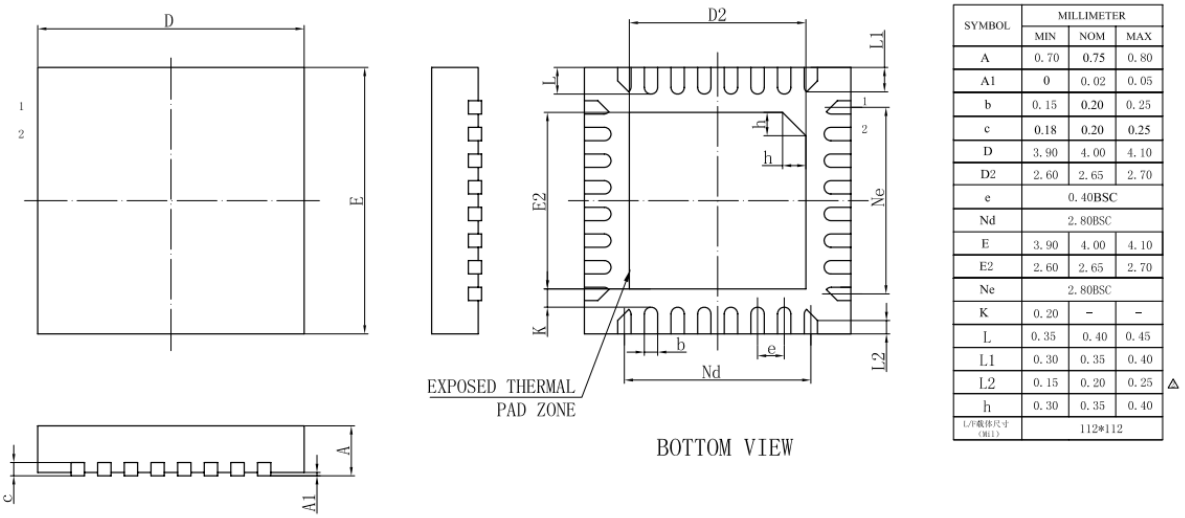
Enhanced Data Rate **Table 2-11**

Parameter		Min	Typ	Max	Unit	Test Conditions
Sensitivity		-95	-94		dBm	25℃, Power Supply VBAT=3.7V 2441MHz 2DH5
Co-channel Interference Rejection			10		dB	
Adjacent Channel Interference Rejection	+1MHz		-4		dB	
	-1MHz		-3		dB	
	+2MHz		-39		dB	
	-2MHz		-29		dB	
	+3MHz		-45		dB	
	-3MHz		-23		dB	

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3、Package Information

3.1 QFN32_4.0x4.0



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.60	2.65	2.70
e	0.40BSC		
Nd	2.80BSC		
E	3.90	4.00	4.10
E2	2.60	2.65	2.70
Ne	2.80BSC		
K	0.20	–	–
L	0.35	0.40	0.45
L1	0.30	0.35	0.40
L2	0.15	0.20	0.25
h	0.30	0.35	0.40
L/F载体尺寸 (mil)	112*112		

Figure 3-1 JL7016C Package

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4、Revision History

Date	Revision	Description
2022.04.15	V1.0	Initial Release

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